IN THE CLAIMS

78. (New) A method for placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside, wherein a circuit density of a ratio of total cells area to total available site area is one hundred percent;

performing a coarse placement process that assigns initial locations to the cells; and

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, wherein no two cells are overlapping, and wherein each cell is assigned to a group of legal sites so that each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area.

79. (New) The method of Claim 78, wherein the detailed placement process runs in linear time.

80. (New) The method of Claim 78, wherein the detailed placement process further comprises the step of using a dynamic programming technique to perform the swapping of cells between the pairs of rows.

81. (New) The method of Claim 78, wherein a look-ahead parameter is used to control usages of cell swapping between pairs of rows.

82. (New) The method of Claim 78, wherein the detailed placement process further comprises pruning a search space during using a dynamic programming technique to perform the swapping of cells between the pairs of rows.

83. (New) The method of Claim 82, wherein the pruning step is controlled as a function of a gap count.

84. (New) The method of Claim 78, wherein the detailed placement process uses a subroutine that finds an optimal legal cell location assignment for a single row in an absence of blockages.

85. (New) The method of Claim 78, wherein the detailed placement process further comprises the step of assigning an initial cell location based on a result of the coarse placement process.

86. (New) The method of Claim 85, wherein the coarse placement process uses conjugate gradient method.

87. (New) The method of Claim 85, wherein the detailed placement process further comprises optimizing a y-location of the cells during initial cell location assignment.

88. (New) The method of Claim 87, wherein the optimizing step is performed through a dynamic programming technique.

89. (New) The method of Claim 88, wherein the detailed placement process further comprises the step of performing a greedy cleanup phase.

90. (New) A method for placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification to the placement area; and

using a dynamic programming technique to perform a swapping of cells between the pairs of rows based on the cost function.

91. (New) The method of Claim 90, wherein the detailed placement process runs in linear time.

92. (New) The method of Claim 90, wherein a circuit density of a ratio of total cell area to total available site area is one hundred percent.

93. (New) The method of Claim 90, wherein a look-ahead parameter is used to control usages of the swapping of cells between pairs of rows.

94. (New) The method of Claim 90, wherein the detailed placement process further comprises the step of pruning a search space during the dynamic programming process.

95. (New) The method of Claim 94, wherein the pruning step is controlled as a function of a gap count.

96. (New) The method of Claim 90, wherein the detailed placement process uses a subroutine that finds an optimal legal cell location assignment for a single row in an absence of blockages.

97. (New) The method of Claim 90, wherein the detailed placement process further comprises the step of assigning an initial cell location based on a result of the coarse placement process.

98. (New) The method of Claim 97, wherein the coarse placement process uses conjugate gradient method.

99. (New) The method of Claim 97, wherein the detailed placement process further comprises the step of optimizing a y-location of the cells during the initial cell location assignment.

100. (New) The method of Claim 99, wherein the optimizing step is performed through the dynamic programming technique.

101. (New) The method of Claim 100, wherein the detailed placement process further comprises the step of performing a greedy cleanup phase.

102. (New) A method of placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells according to conjugate gradient process; and

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area.

103. (New) The method of Claim 102, wherein the detailed placement process runs in linear time.

104. (New) The method of Claim 102, wherein a circuit density of a ratio of total cell area to total available site area is one hundred percent.

105. (New) The method of Claim 102, wherein a look-ahead parameter is used to control usages of the swapping of cells between pairs of rows.

106. (New) The method of Claim 102, wherein the detailed placement process further comprises the step of pruning a search space during a dynamic programming process for the swapping of cells between the pairs of rows based on the cost function.

107. (New) The method of Claim 106, wherein the pruning step is controlled as a function of a gap count.

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108. (New) The method of Claim 102, wherein the detailed placement process uses a subroutine that finds an optimal legal cell location assignment for a single row in an absence of blockages.

109. (New) The method of Claim 108, wherein the detailed placement process further comprises the step of assigning an initial cell location based on a result of the coarse placement process.

110. (New) The method of Claim 109, wherein the detailed placement process further comprises the step of optimizing a y-location of the cells during the initial cell location assignment.

111. (New) The method of Claim 110, wherein the optimizing step is performed through the dynamic programming technique.

113. (New) The method of Claim 112, wherein the detailed placement process further comprises the step of performing a greedy cleanup process.

114. (New) A method of placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

using a subroutine that legalizes a single row optimally according to a sum of squares objective in linear, quadratic, or polynomial run time.

115. (New) A method for placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

using a subroutine that legalizes a single row optimally for a given fixed cell ordering in linear, quadratic, or polynomial run time.

116. (New) A method of placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

legalizing a single row optimally using a dynamic programming technique for the swapping of cells between the pairs of rows based on the cost function.

117. (New) A method for placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby

allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

using a subroutine that legalizes two rows optimally according to a sum of squares objective in quadratic or polynomial run time.

118. (New) A method of placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

using a subroutine that legalizes two rows optimally for a given fixed cell ordering in quadratic or polynomial run time.

119. (New) A method of placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

legalizing two row optimally using a dynamic programming technique for the swapping of cells between the pairs of rows based on the cost function.

120. (New) A method for placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

using a subroutine that legalizes a pair of rows optimally according to y-displacement metric in quadratic or polynomial time.

121. (New) A method for placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby

allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

using a subroutine that legalizes N rows optimally according to a y-displacement metric in quadratic or polynomial run time.